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Approved for use through 09/30/2000. OMB 0651-0033
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

JC759 U.S. PTO 01/20/00

REISSUE PATENT APPLICATION TRANSMITTAL

Address to:
Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

Attorney Docket No.	93-C-078C1 (1678-10)
First Named Inventor	Loi Nguyen
Original Patent Number	5,710,461
Original Patent Issue Date (Month/Day/Year)	January 20, 1998
Express Mail Label No.	EK434158406US

APPLICATION FOR REISSUE OF: *(check applicable box)* [X] *Utility Patent* [ ] *Design Patent* [ ] *Plant Patent*

APPLICATION ELEMENTS

1. [ ] * Fee Transmittal Form *(PTO/SB/56)* *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification and Claims (*amended, if appropriate*)
3. [ ] Drawing(s) *(proposed amendments, if appropriate)*
4. [X] Reissue Oath / Declaration (original or copy) *(37 C.F.R. § 1.175)(PTO/SB/51 or 52)*
5. Original U.S. Patent
   - [X] Offer to Surrender Original Patent *(37 C.F.R. § 1.178) (PTO/SB/53 or PTO/SB/54)*
   - *or*
   - [ ] Ribboned Original Patent Grant
   - [ ] Affidavit / Declaration of Loss *(PTO/SB/55)*
6. Original U.S. Patent currently assigned? [X] Yes [ ] No
   (If Yes, check applicable box(es))
   - [X] Written Consent of all Assignees *(PTO/SB/53 or 54)*
   - [X] 37 C.F.R. § 3.73(b) Statement [ ] Power of Attorney

ACCOMPANYING APPLICATION PARTS

7. [ ] Foreign Priority Claim *(35 U.S.C. 119)* *(if applicable)*
8. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
9. [ ] English Translation of Reissue Oath/Declaration *(if applicable)*
10. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
11. [X] Preliminary Amendment
12. [X] Return Receipt Postcard *(MPEP 503)* *(Should be specifically itemized)*
13. [X] Other: Certificate of Express Mailing

NOTE FOR ITEMS 1 & 10: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

14. CORRESPONDENCE ADDRESS

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Signature	Paul F. Rusyn	*Date*	1/20/2000

EXPRESS MAIL NO. EK434158410US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Reissue Patent Application:

Applicant	:	Loi Nguyen and Ravishankar Sundaresan
Assignee	:	STMicroelectronics, Inc.
Filed	:	
Title	:	SRAM CELL FABRICATION WITH INTERLEVEL DIELECTRIC PLANARIZATION
Docket No.	:	1678-20

Corresponding Issued U.S. Patent:

Patent No.	:	5,710,461
Issued	:	January 20, 1998
Appln. No.	:	08/781,429
Filed	:	January 10, 1997
Examiner	:	A. Williams
Art Unit	:	2508

BOX PATENT APPLICATIONS
Assistant Commissioner for Patents
Washington, DC 20231

OFFER TO SURRENDER THE ORIGINAL PATENT

Sir:

STMicroelectronics, Inc., owner by assignment of the entire interest in U.S. Letters Patent No. 5,710,461 which is entitled SRAM CELL FABRICATION WITH INTERLEVEL DIELECTRIC PLANARIZATION and issued on January 20, 1998 to STMicroelectronics, Inc., hereby offers to surrender said Letters Patent.

STMicroelectronics, Inc.

____
Date

By:_____________________________
Archie McK. Malone
Executive Vice President
Finance & C.F.O. and Treasurer

A/RE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

01-24-00

Original Patent

Patentee: Loi Nguyen and Ravishankar Sundaresan

Patent No.: 5,710,461

Title: SRAM CELL FABRICATION WITH INTERLEVEL DIELECTRIC PLANARIZATION

Issued: January 20, 1998

Atty Dk No.: 93-C-078C1

JC530 U.S. PTO 09/488686 01/20/00

JC759 U.S. PTO 01/20/00

Reissue Application

Applicant: Loi Nguyen and Ravishankar Sundaresan

Serial No.:

Title: SRAM CELL FABRICATION WITH INTERLEVEL DIELECTRIC PLANARIZATION

Filing Date:

Atty Dk No.: 93-C-078C1 (1678-20)

CERTIFICATE OF MAILING OR TRANSMISSION

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Stephanie Cox

Signature

Enclosures:

- Reissue Patent Application Transmittal
- Reissue Application by the Assignee, Offer to Surrender Patent (not signed)
- Certificate Under 37 C.F.R. 3.73(b) (not signed)
- Assent of Assignee (not signed)
- Reissue Application Declaration by the Inventors (not signed)
- First Preliminary Amendment
- Copy of Patent No. 5,710,461 (regular)
- Copy of Patent No. 5,710,461 (in one column form)
- Return postcard

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Original Patent

Patentee:	Nguyen et al.
Patent No.:	5,710,461
Title:	SRAM CELL FABRICATION WITH INTERLEVEL DIELECTRIC PLANARIZATION
Issued:	January 20, 1998
Docket No.:	93-C-078C1

Reissue Application

Applicant:	Nguyen et al.
Application. No.:	
Title:	SRAM CELL FABRICATION WITH INTERLEVEL DIELECTRIC PLANARIZATION
Docket No.:	93-C-078C1-RE (1678-20)
Date:	January 20, 2000

BOX REISSUE
Assistant Commissioner for Patents
Washington, DC 20231

CERTIFICATE OF MAILING OR TRANSMISSION
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Stephanie Cox
Signature

FIRST PRELIMINARY AMENDMENT

Sir:

Please amend the above-identified reissue application as follows:

In the Drawings:

The Applicant respectfully requests the Examiner to transfer Figures 1-7 from the file of issued U.S. Patent No. 5,710,461 ('461 patent) to the present reissue application file.

In the Claims:

Please amend the claims as follows:

1. An integrated circuit SRAM cell, comprising:

a substrate which includes at least one substantially monolithic body of semiconductor material;

a first patterned thin-film layer comprising polysilicon;

a second patterned thin-film layer comprising polysilicon and overlying said first thin-film layer, said second layer being doped to provide high conductivity;

a patterned interlevel dielectric overlying portions of said first and second thin-film layers, said interlevel dielectric including multiple independently planarized layers of dielectric material therein, said multiple independently planarized layers including a lower portion of a spin-on glass a middle portion of a dielectric material which is not spin-on glass, and an upper portion of spin-on glass;

a third patterned thin-film layer comprising [substantially undoped] polysilicon having a very high resistivity;

wherein said first patterned thin-film layer is configured to provide transistor gates, and said first and second thin-film layers are interconnected to provide an array of latches, and said third thin-film layer overlies said patterned interlevel dielectric and is interconnected through contact holes with said first and second layers to provide resistive loads for each said latch.

7. An integrated circuit SRAM cell, comprising:

first and second overlaid thin-film conductor layers, each comprising clad polysilicon[;], at least one of said conductor layers being capacitively coupled to substantially monolithic semiconductor material to define field-effect transistor channels therein;

a patterned interlevel dielectric overlying portions of said second thin-film layer, and including multiple independently planarized layers of dielectric material therein, said multiple

independently planarized layers of dielectric material including at least three different layers of dielectric material, with at least two of said layers of dielectric material being independently planarized layers of spin-on glass;

a third patterned thin-film layer comprising [substantially undoped] polysilicon having a very high resistivity, and lying on a substantially planar top surface of said patterned interlevel dielectric;

wherein said [first patterned thin-film layer is configured to provide transistor gates, and lust] first and second thin-film layers are interconnected to provide an array of latches, and said third thin-film layer overlies said patterned interlevel dielectric and is interconnected through contact holes with said first and second layers to provide passive loads for respective ones of said latches.

12. An integrated circuit SRAM cell, comprising:

at least one patterned thin-film conductor layer comprising polysilicon and being capacitively coupled to substantially monolithic semiconductor material to define field-effect transistor channels therein;

a patterned interlevel dielectric overlying said at least one patterned thin-film conductor layer[s], and including multiple independently planarized layers of dielectric materials therein, said multiple independently planarized layers of dielectric material including at least three different layers of dielectric material, with at least two of said layers of dielectric material being independently planarized layers of spin-on glass;

an additional patterned thin-film layer comprising [substantially intrinsic] polysilicon, and lying on a substantially planar top surface of said patterned interlevel dielectric;

wherein said at least one patterned thin-film conductor layer [are] is interconnected to provide an array of latches, and said additional thin-film layer overlies said patterned interlevel dielectric and is interconnected through contact holes with said conductor layers to provide passive loads for respective ones of said latches.

Please add the following new claims to the reissue application:

19. The integrated circuit SRAM cell of claim 1 wherein the third patterned thin-film layer comprises substantially undoped polysilicon.

20. The integrated circuit SRAM cell of claim 19 wherein the substantially undoped polysilicon comprises intrinsic polysilicon.

21. The integrated circuit SRAM cell of claim 1 wherein the third patterned thin-film layer comprises a polysilicon layer doped with chlorine.

22. The integrated circuit SRAM cell of claim 7 wherein the third patterned thin-film layer comprises substantially undoped polysilicon.

23. The integrated circuit SRAM cell of claim 22 wherein the third patterned thin-film layer comprises intrinsic polysilicon.

24. The integrated circuit SRAM cell of claim 7 wherein the third patterned thin-film layer comprises a polysilicon layer doped with chlorine.

25. The integrated circuit SRAM cell of claim 12 wherein the third patterned thin-film layer comprises substantially intrinsic polysilicon.

26. An integrated circuit SRAM cell formed in a semiconductor substrate, a plurality of active transistor regions being formed in the substrate, the SRAM cell comprising:

a first conductive layer disposed on the semiconductor substrate, the first conductive layer being coupled to the active transistor regions to form a plurality of respective control nodes for respective transistors in the substrate;

a second conductive layer disposed over the first conductive layer, the second conductive layer being coupled to the first conductive layer and to active transistor regions to interconnect groups of transistors and thereby form respective data latches;

a plurality of planarizing layers disposed on the second conductive layer;

an insulating layer disposed on a top one of the planarizing layers; and

a third conductive layer formed on the insulating layer, the third conductive layer being coupled to the data latches to form respective resistive loads for the respective latches.

27. The integrated circuit SRAM cell of claim 26 wherein the plurality of planarizing layers includes a first spin-on-glass layer disposed on the second polysilicon layer, an oxide layer disposed on the first spin-on-glass layer, and a second spin-on-glass layer disposed on the oxide layer.

28. The integrated circuit SRAM cell of claim 26 wherein each of the conductive layers comprises a suitably doped polysilicon layer.

29. The integrated circuit SRAM cell of claim 26 wherein the a first conductive layer comprises a first polysilicon layer and a cladding layer formed on the first polysilicon layer.

30. The integrated circuit SRAM cell of claim 29 wherein the cladding layer comprises tantalum silicide.

31. The integrated circuit SRAM cell of claim 26 wherein the a second conductive layer comprises a second polysilicon layer and a cladding layer formed on the second polysilicon layer.

32. The integrated circuit SRAM cell of claim 31 wherein the cladding layer comprises tantalum silicide.

33. The integrated circuit SRAM cell of claim 26 wherein the insulating layer comprises an undoped oxide layer.

34. The integrated circuit SRAM cell of claim 26 wherein the third conductive layer comprises intrinsic polysilicon.

REMARKS

Claims 1-34 are pending in this broadening reissue application. The Applicant has amended claims 1, 7, and 12 to correct one of the errors described in the reissue declaration and discussed below, and has added new claims 19-34.

The Applicants have amended original independent claims 1, 7, and 12 to remove a limitation that resulted in Applicants claiming less than they had a right to claim. As set forth in the Reissue Declaration, original independent claims 1 and 7 as issued recite "a third patterned thin-film layer comprising substantially undoped polysilicon having a very high resistivity," and original independent claim 12 as issued recites "an additional patterned thin-film layer comprising substantially intrinsic polysilicon." Each of these thin film layers corresponds to layer in which resistors for Static Random Access Memory (SRAM) cells are formed. Regarding these resistors, the specification expressly states in column 4, lines 46-51, that "[a]lthough the resistors are formed from intrinsic polysilicon in the presently preferred embodiment, it will be recognized that a slight amount of doping may be desirable to stabilize the characteristics of this material. For example, this material may be doped with chlorine, or may be SIPOS (containing a large fraction of oxygen)." Thus, the "substantially undoped" language unduly limits the scope of original claims 1 and 7, and the same is true of the "substantially intrinsic" language in original claim 12. Accordingly, the language "substantially undoped" has been deleted in amended claims 1 and 7 and the language "substantially intrinsic" has been deleted in amended claim 12. Newly added dependent claims 19-23 recite further limitations of the layer set forth in the corresponding independent claim that was broadened through the previously discussed amendments.

In view of the foregoing, original independent claims 1, 7, and 12 as amended, original dependent claims 2-6, 8-11, and 13-19, and newly added claims 19-34 are in condition for allowance, and allowance is requested.

If the Examiner believes that a phone interview would be helpful, he is respectfully requested to contact the Applicants' attorney, Paul F. Rusyn, at (425) 455-5575.

Please note that the firm, GRAYBEAL JACKSON HALEY LLP, of Applicants' attorney has recently moved to : 155 – 108th Avenue NE, Suite 350, Bellevue, Washington 98004-5901. The telephone and facsimile numbers remain the same. Please send all future communications to that address.

Respectfully submitted,

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Enclosures

SRAM CELL FABRICATION WITH INTERLEVEL DIELECTRIC PLANARIZATION

This application is a continuation of application No. 08/328,736, filed Oct. 25, 1995, which was abandoned upon the filing herein which is a divisional of 08/49,338, filed Dec. 17, 1993, now U.S. Pat. No. 5,395,785.

BACKGROUND AND SUMMARY OF THE INVENTION

The present invention relates to integrated circuit fabrication methods and structures, and particularly to integrated circuits with minimum linewidths below one-half micron.

Background: Planarization

As the degree of integration has advanced, it has become increasingly apparently that it is desirable to minimize the topographical excursion of the surface at each level, especially the upper levels. To accomplish this, various planarization schemes have been used to planarize the interlevel dielectric. Some of these include Chemical-Mechanical-Polishing (CMP), use of Permanent Spin-on-glass (left in place in the final chip), and Sacrificial Etchback Spin-on-glass (SOG).

Spin-on glass deposition is an example of a "sol-gel" process, which has been used in the semiconductor industry for many years. The unprocessed spin-on glass material (available in numerous formulations) is a fluid material (actually a gel). After the liquid material is coated onto the face of a wafer, the wafer is rotated at high speed to throw off the excess material. The surface tension and adhesion of the material provides a flat (planarized) surface with a controlled thickness. The liquid material is then baked, to drive off solvents and provide a stable solid silicate glass. See generally, e.g., Dauksher et al., "Three 'low Dt' options for planarizing the pre-metal dielectric on an advanced double poly BiCMOS process," 139 J.ELECTROCHEM.SOC. 532–536 (1992), which is hereby incorporated by reference.

Background: SRAM Cell Operation

One of the two most common types of SRAM cell is the "4-T" cell, which uses resistive loads. FIG. 7 is a circuit diagram of such a cell (a 4-transistor 2-resistor MOS SRAM cell). In the example shown, the numbering of the bitlines and wordlines indicates that this cell would be in the n-th row and m-th column of an array (or subarray) of memory cells. In this cell, NMOS driver transistors D1 and D2, loaded by resistors R1 and R2, are cross-connected to form a latch. Pass transistors PT1 and PT2 are both accessed by a respective wordline WL_n, to connect the two complementary nodes of the latch to a respective complementary pair of bitlines BL_m and BL_m* when wordline WL_n goes high. Thus, in read mode, when wordline WL_n goes high, whichever one of the driver transistors (D1 or D2) is ON will pull down one of the bitlines (BL_m or BL_m*), producing a data signal which can be read. In write mode, the bitlines will be clamped by strong drivers, and the pass transistors PT1 and PT2 will pass enough current to change the state of the latch to correspond to the bitline voltages.

In such a memory cell, the resistors R1 and R2 must pass enough current to offset the leakage currents which tend to discharge the high node of the latch. These resistors are conventionally made from nearly intrinsic polysilicon, and therefore tend to have very high resistance values (which may range from many gigaohms up to teraohms). Unfortunately, the resistivity of such polysilicon is fairly

variable, and an excessive value for the resistors may cause the cell to lose data under high-temperature conditions. An excessively low value for the polysilicon resistor may lead to excess static power consumption. Thus, precise control of the resistor values would be highly desirable.

Innovative SRAM Structure and Process

This disclosure describes an improved method of four transistor SRAM cell fabrication, wherein planarization is performed before metal formation (and actually before resistor formation). The pre-metal planarization utilizes a sandwich structure comprising permanent SOG, undoped glass, and permanent SOG. The undoped glass is used as a buffer layer between two layers of spin-on-glass to prevent SOG cracks. The double SOG spin enhances the degree of planarization.

The disclosed inventions thus provide the advantages of reduced topography at the poly-2 level, and hence more accurate patterning of the poly resistors, and hence a reduced poly-R resistance value by shortening resistor length (less surface contour due to better planarity). This provides more precise manufacturing control which can be used to set speed and power more reliably.

BRIEF DESCRIPTION OF THE DRAWING

The present invention will be described with reference to the accompanying drawings, which show important sample embodiments of the invention and which are incorporated in the specification hereof by reference, wherein:

FIG. 1 shows a section of a standard 1 Mb SRAM, and

FIG. 2 shows a modification of the structure according to the disclosed innovations.

FIG. 3 is a micrograph of a plan view of a standard structure, and

FIG. 4 is a micrograph of a plan view of a comparable structure made according to the disclosed inventions.

FIG. 5 is a micrograph of a section view of a standard structure, and

FIG. 6 is a micrograph of a section view of a comparable structure made according to the disclosed inventions.

FIG. 7 is a circuit diagram of a 4-transistor 2-resistor MOS SRAM cell.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The numerous innovative teachings of the present application will be described with particular reference to the presently preferred embodiment. However, it should be understood that this class of embodiments provides only a few examples of the many advantageous uses of the innovative teachings herein. In general, statements made in the specification of the present application do not necessarily delimit any of the various claimed inventions. Moreover, some statements may apply to some inventive features but not to others.

After completion of CMOS transistor formation (and local interconnect formation in the poly-2 layer, if desired), a standard process flow (as shown in FIG. 1) would deposit e.g. 1KÅ of undoped oxide, spin on e.g. 1.5KÅ of SOG, deposit e.g. 1KÅ of undoped oxide, deposit and etch a second polysilicon layer to form polysilicon resistors, and then proceed with contact and metal formation.

In the innovative process embodiments described, fabrication of the lower poly level(s) is instead followed by:

deposition of undoped oxide (not separately shown) to e.g. 1KÅ;

Spin-on and cure of SOG **150** (e.g. P112 from Allied) to e.g. 1.5KÅ;

deposition of additional undoped oxide **152** to e.g. 500Å;

spin-on and cure of additional SOG **155** (e.g. P112 from Allied) to e.g. 1.5KÅ;

deposition of additional undoped oxide **160** to e.g. 1KÅ;

contact etch (if desired); and

deposition and patterning of a top level **330** of polysilicon, to form planar resistors.

Processing then continues conventionally with contact and metal formation.

The disclosed inventions thus provide the advantages of reduced topography at the top poly level, and hence more accurate patterning of the poly resistors. A comparison of FIGS. **3** and **4** illustrates this advantage: FIG. **3** is a micrograph of a plan view of a standard structure, and FIG. **4** is a micrograph of a plan view of a comparable structure made according to the disclosed inventions.

The disclosed inventions also provide the advantages of reduced poly-R resistance value by shortening the effective resistor length (since the reduced surface contour leads to better planarity). A comparison of FIGS. **5** and **6** illustrates this advantage: FIG. **5** is a micrograph of a section view of a standard structure, and FIG. **6** is a micrograph of a section view of a comparable structure made according to the disclosed inventions. This in turn can be used to provide faster memory operation, since the load resistors can have a greater pullup capability for the same layout area. That is, the reliably greater pullup capability of the load resistors means that the driver and pass transistor dimensions can be selected for faster operation, without risk of upsetting the latch when the pass transistors turn on.

FIG. **1** shows a cross-section through a partially fabricated triple-poly 4-T SRAM cell, which has been partially fabricated according to conventional methods. (Metallization has been omitted for clarity.) Substrate **100** includes multiple IGFET transistors **110** separated by field oxide **120**. The gates of these NMOS transistors are provided by a first polysilicon layer **130**, which is clad, in the presently preferred embodiment, with a tantalum silicide layer **132**. (This composite layer **130/132** is referred to herein as the "poly-1" layer.) The poly-1 layer **130/132** provides gate electrodes for the transistors **110**. (The gate oxide which separates the transistor gates from the substrate is too thin, e.g. 100–150 Å, to be shown in this drawing.) Sidewall spacers **112** are self-aligned to the poly-1 layer **130/132**.

A second layer of polysilicon **230** (which, in the presently preferred embodiment, is also clad with a respective tantalum silicide layer **232**) provides local interconnect within the cell. (This composite layer **230/232** is referred to herein as the "poly-2" layer.) A permanent SOG layer **150**, overlaid by an undoped oxide layer **160**, provides some planarization over the poly-2 layer. (An additional layer of undoped oxide, which is omitted from this drawing for simplicity, underlies the permanent SOG layer **150**.) A shared contact, in the presently preferred embodiment, provides contacts from poly-1 and poly-2 to active.

A third polysilicon layer **330**, made of substantially intrinsic polysilicon, provides the polysilicon resistors. (This layer **330** is referred to herein as the "poly-R" layer.) Another shared contact is used to provide contact from this layer to the poly-2 (and poly-1) layers.

FIG. **2** shows a cross-section through a partially fabricated triple-poly 4-T SRAM cell, which has been partially fabricated according to the disclosed innovative methods.

Elements **100**, **110**, **120**, **130**, **132**, **112**, **230**, **232**, and **150** all are generally the same as the corresponding elements in FIG. 1. However, in the structure of FIG. 2, an additional layer of undoped oxide **152** overlies the SOG **150**, and an additional planarizing layer **155** of permanent SOG (e.g. P114 from Allied) overlies the oxide layer **152**.

This results in a structure wherein the topographic excursion H_2 of the more planar poly-R layer **330'0** provided by the disclosed innovations is much less than the topographic excursion H_1 of the poly-R layer **330** of the more conventional structure shown in FIG. 1.

The disclosed inventions also provide the advantages of reduced topographical excursion for the contact and metal-1 layer, and hence reduced requirements for planarization after the poly-2 layer.

The resistors R1 and R2 are preferably laid out to have a target resistance value of about 1TΩ, but of course this value can be adjusted, by appropriate layout changes, to adjust for speed and power requirements as needed. However, the disclosed innovations permit the resistor value to be specified with greater precision.

Further Modifications and Variations

It will be recognized by those skilled in the art that the innovative concepts disclosed in the present application can be applied in a wide variety of contexts. Moreover, the preferred implementation can be modified in a tremendous variety of ways. Accordingly, it should be understood that the modifications and variations suggested below and above are merely illustrative. These examples may help to show some of the scope of the inventive concepts, but these examples do not nearly exhaust the full scope of variations in the disclosed novel concepts.

While the inventions have been described with primary reference to a 4-T SRAM cell, it will be readily recognized that these inventions can also be applied to other integrated circuits which use resistive loads. Note, however, that the disclosed innovations would not be as applicable to processes which include floating-gate memory cells or poly-to-poly capacitors in the top poly level, since the planarization provided by the disclosed inventions would require additional process complexity to achieve the close coupling from the top poly level to the next lower poly level.

Although the presently preferred embodiment actually uses a triple-poly cell layout, it will be readily recognized that the disclosed ideas can also be adapted for use in a double-poly resistive-load SRAM cell.

Although the resistors are formed from intrinsic polysilicon in the presently preferred embodiment, it will be recognized that a slight amount of doping may be desirable to stabilize the characteristics of this material. For example, this material may be doped with chlorine, or may be SIPOS (containing a large fraction of oxygen).

As will be recognized by those skilled in the art, the innovative concepts described in the present application can be modified and varied over a tremendous range of applications, and accordingly the scope of patented subject matter is not limited by any of the specific exemplary teachings given.

What is claimed is:

1. An integrated circuit SRAM cell, comprising:

a substrate which includes at least one substantially monolithic body of semiconductor a first patterned thin-film layer comprising polysilicon;

a second patterned thin-film layer comprising polysilicon and overlying said first thin-film layer, said second layer being doped to provide high conductivity;

a patterned interlevel dielectric overlying portions of said first and second thin-film layers, said interlevel dielec-

tric including multiple independently planarized layers of dielectric material therein, said multiple independently planarized layers including a lower portion of a spin-on glass a middle portion of a dielectric material which is not spin-on glass, and an upper portion of spin-on glass;

a third patterned thin-film layer comprising substantially undoped polysilicon having a very high resistivity;

wherein said first patterned thin-film layer is configured to provide transistor gates, and said first and second thin-film layers are interconnected to provide an array of latches, and said third thin-film layer overlies said patterned interlevel dielectric and is interconnected through contact holes with said first and second layers to provide resistive loads for each said latch.

2. The integrated circuit of claim 1, wherein said first thin-film layer also comprises a silicide cladding.

3. The SRAM cell of claim 1, wherein said interlevel dielectric comprises two layers of spin-on glass.

4. The SRAM cell of claim 1, wherein said interlevel dielectric also comprises at least two dielectric layers which are not planarized.

5. The SRAM cell of claim 1, wherein said second interlevel dielectric comprises at least four layers.

6. The SRAM cell of claim 1, wherein said loads each have a resistance value of about 1TΩ.

7. An integrated circuit SRAM cell, comprising:

first and second overlaid thin-film conductor layers, each comprising clad polysilicon; at least one of said conductor layers being capacitively coupled to substantially monolithic semiconductor material to define field-effect transistor channels therein;

a patterned interlevel dielectric overlying portions of said second thin-film layer, and including multiple independently planarized layers of dielectric material therein, said multiple independently planarized layers of dielectric material including at least three different layers of dielectric material, with at least two of said layers of dielectric material being independently planarized layers of pin-on glass;

a third patterned thin-film layer comprising substantially undoped polysilicon having a very high resistivity, and lying on a substantially planar top surface of said patterned interlevel dielectric;

wherein said first patterned thin-film layer is configured to provide transistor gates, and lust and second thin-film layers are interconnected to provide an array of latches, and said third thin-film layer overlies said patterned interlevel dielectric and is interconnected through con-

tact holes with said first and second layers to provide passive loads for respective ones of said latches.

8. The SRAM cell of claim 7, wherein said interlevel dielectric comprises two layers of spin-on glass.

9. The SRAM cell of claim 7, wherein said interlevel dielectric also comprises at least two dielectric layers which are not planarized.

10. The SRAM cell of claim 7, wherein said interlevel dielectric comprises at least four layers.

11. The SRAM cell of claim 7, wherein said loads each have a resistance value of about 1TΩ.

12. An integrated circuit SRAM cell, comprising:

at least one patterned thin-film conductor layer comprising polysilicon and being capacitively coupled to substantially monolithic semiconductor material to define field-effect transistor channels therein;

a patterned interlevel dielectric overlying said thin-film conductor layers, and including multiple independently planarized layers of dielectric material therein, said multiple independently planarized layers of dielectric material including at least three different layers of dielectric material, with at least two of said layers of dielectric material being independently planarized layers of spin-on glass;

an additional patterned thin-film layer comprising substantially intrinsic polysilicon, and lying on a substantially planar top surface of said patterned interlevel dielectric;

wherein said patterned thin-film conductor layer are interconnected to provide an array of latches, and said additional thin-film layer overlies said patterned interlevel dielectric and is interconnected through contact holes with said conductor layers to provide passive loads for respective ones of said latches.

13. The SRAM cell of claim 12, wherein said additional layer comprises SIPOS.

14. The SRAM cell of claim 12, wherein said additional layer comprises polysilicon doped with chlorine.

15. The SRAM cell of claim 12, wherein said interlevel dielectric comprises two layers of spin-on glass.

16. The SRAM cell of claim 12, wherein said interlevel dielectric also comprises at least two dielectric layers which are not planarized.

17. The SRAM cell of claim 12, wherein said interlevel dielectric comprises at least four layers.

18. The SRAM cell of claim 12, wherein said loads each have a resistance value of about 1TΩ.

* * * * *

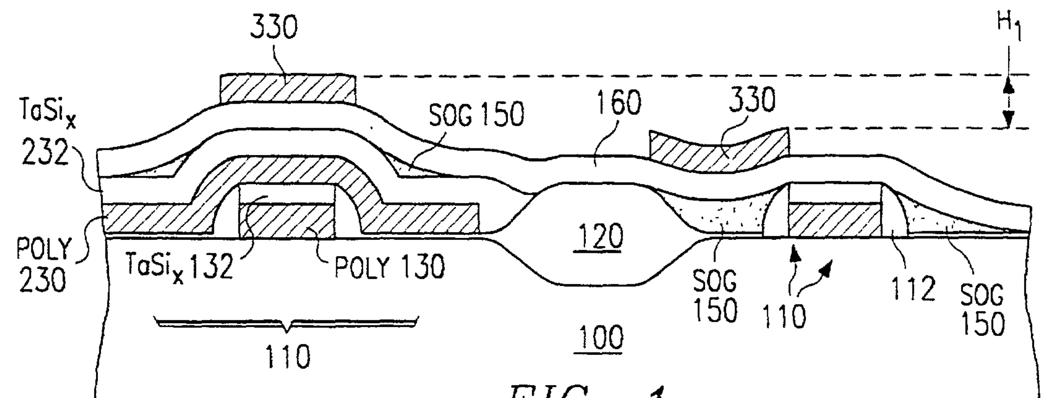

FIG. 1
(PRIOR ART)

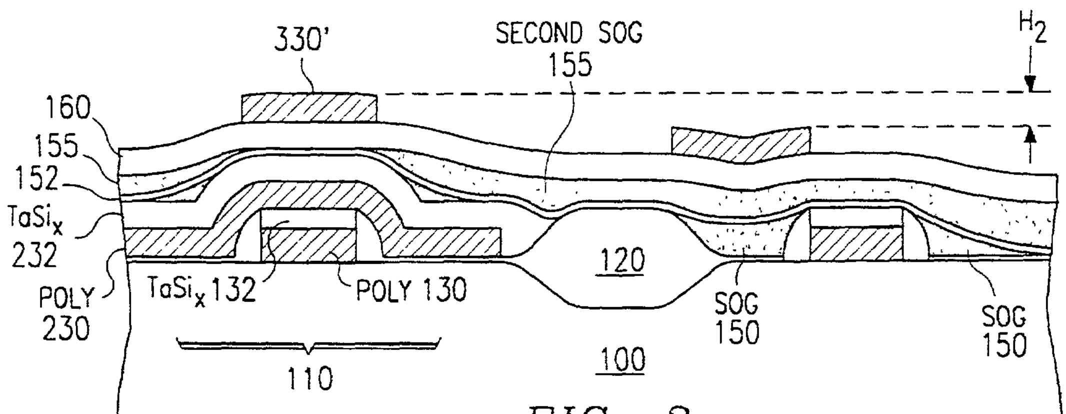

FIG. 2

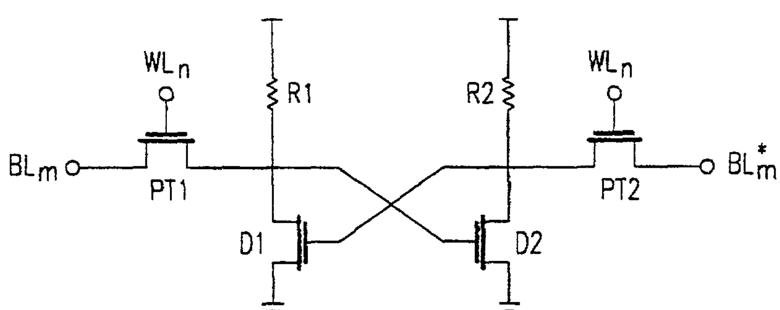

FIG. 7
(PRIOR ART)

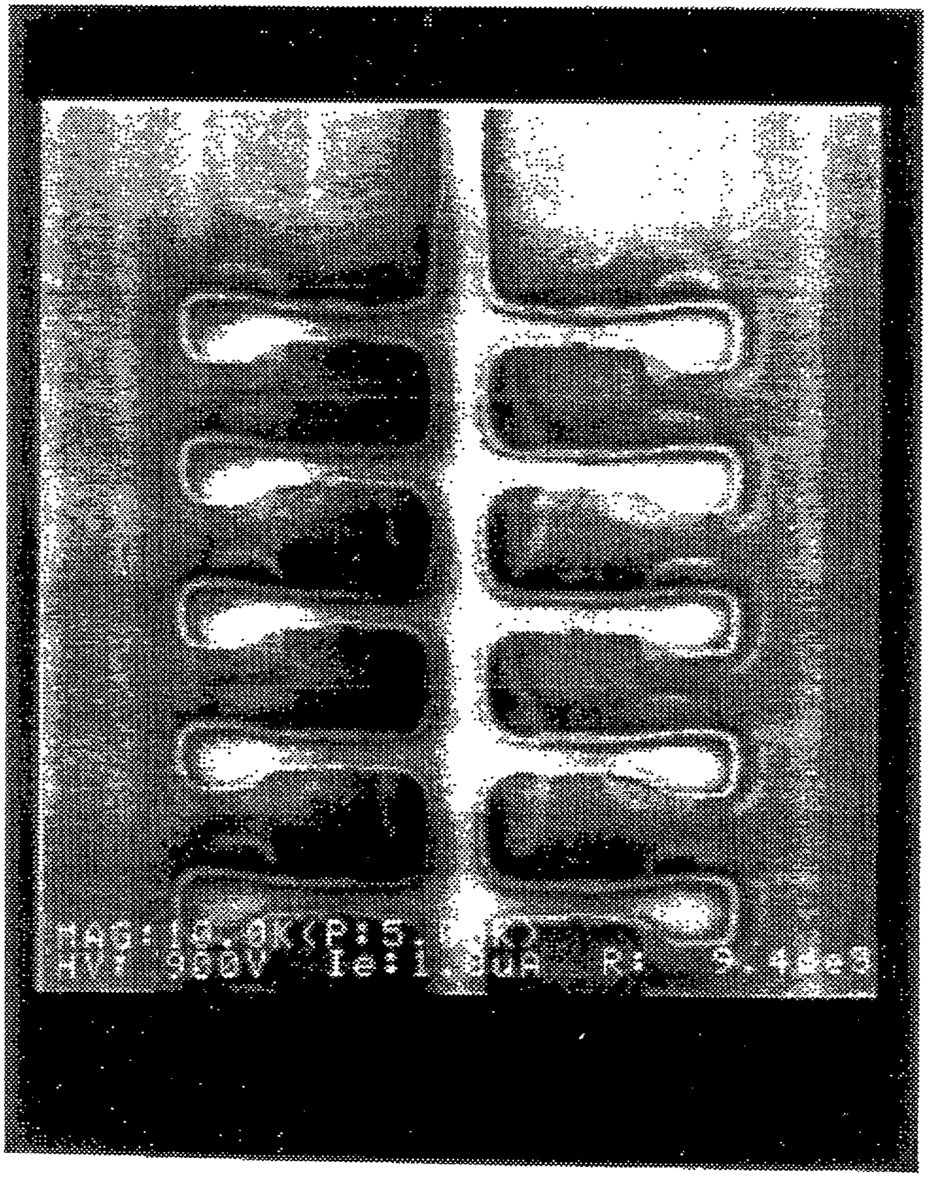

FIG. 3
(PRIOR ART)

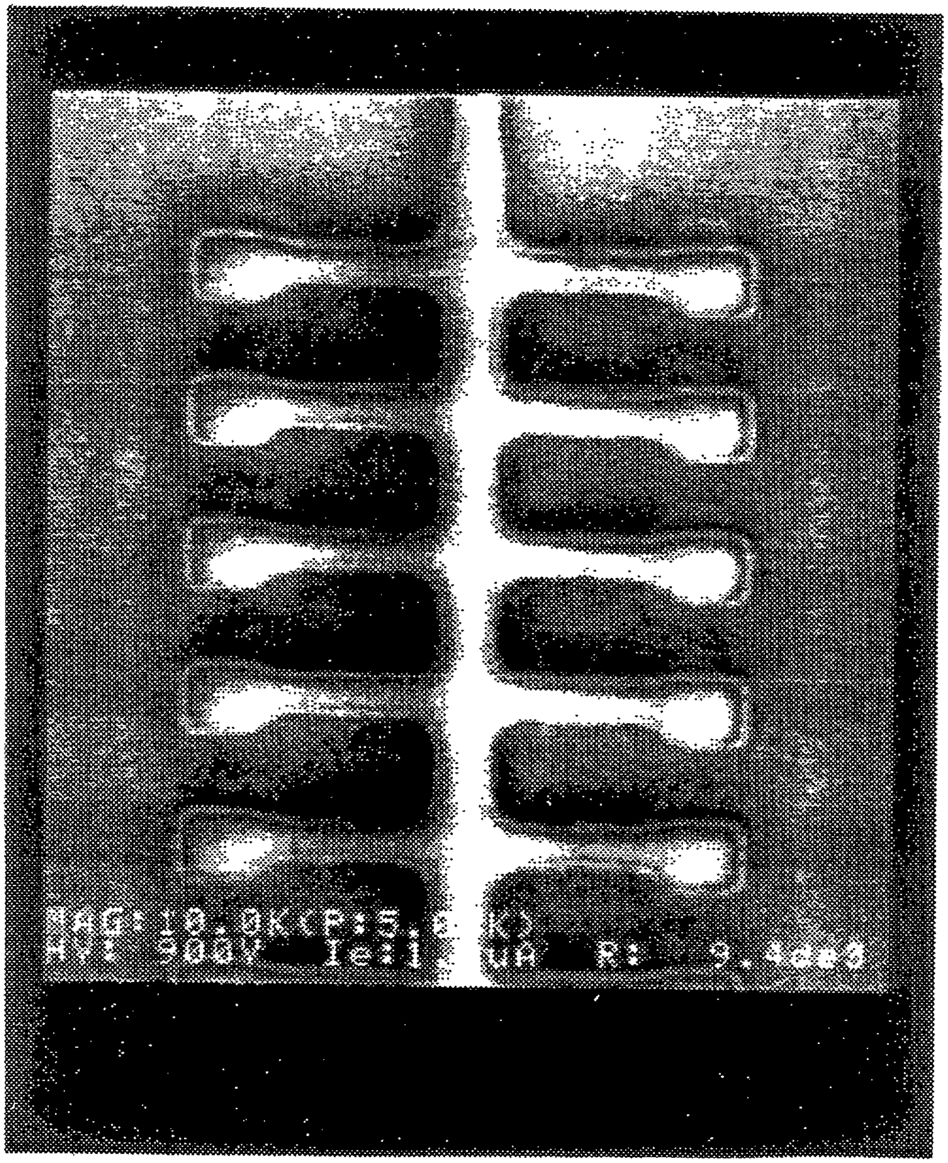

FIG. 4

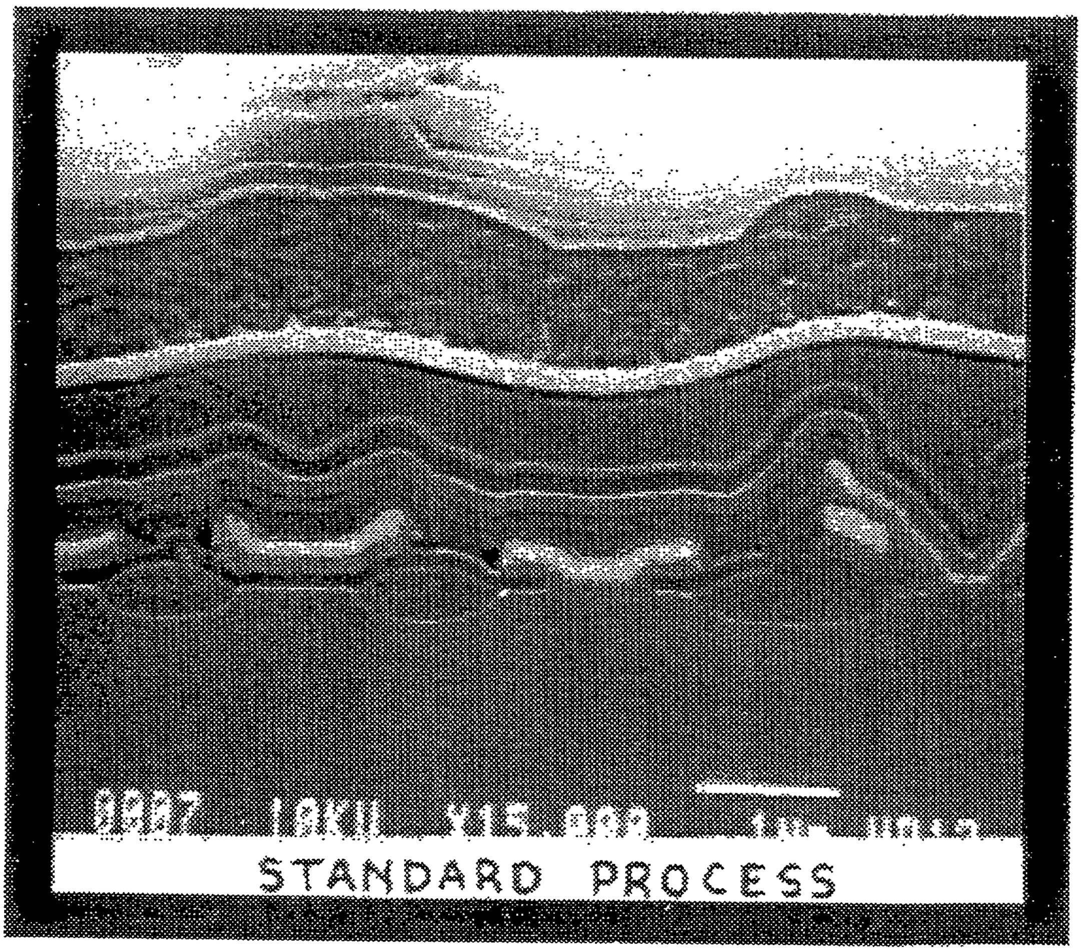

FIG. 5
(PRIOR ART)

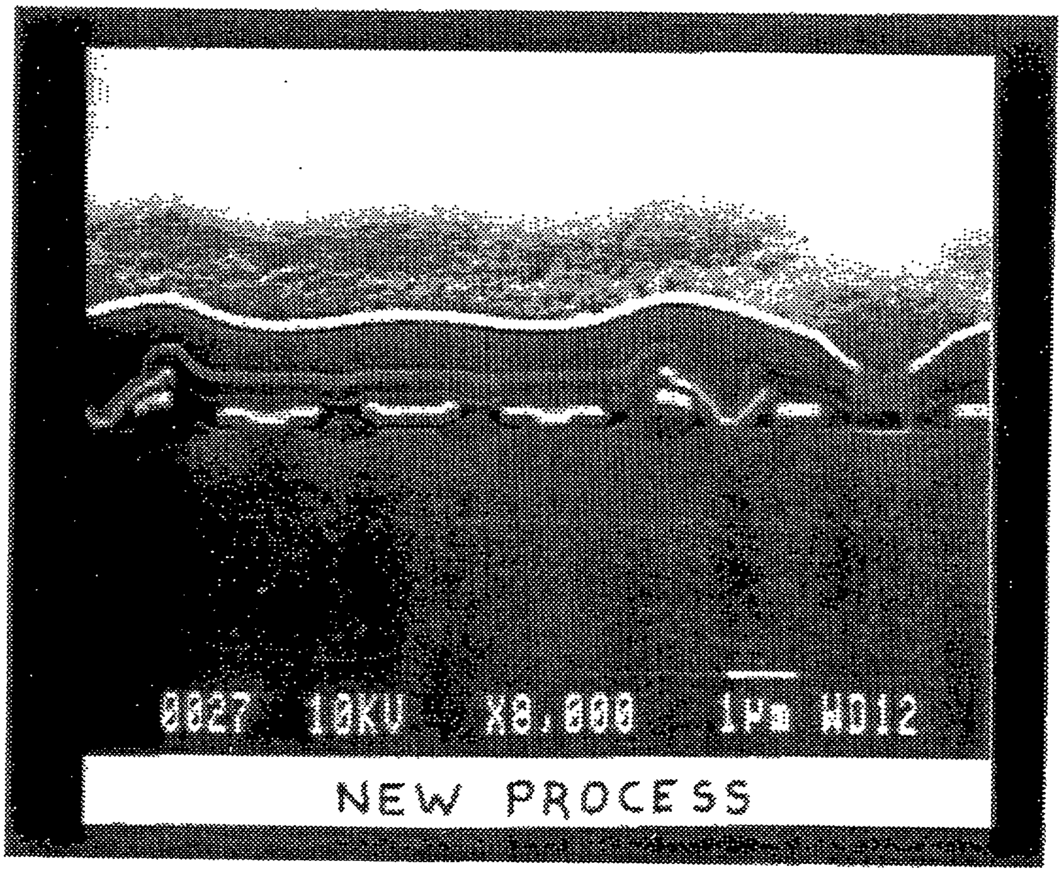

FIG. 6

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Original Patent

Patentee: Loi Nguyen
Ravishankar Sundaresan

Patent No.: 5,710,461

Title: SRAM CELL FABRICATION WITH INTERLEVEL DIELECTRIC PLANARIZATION

Issued: January 20, 1998

Docket No.: 93-C-078C1

Reissue Application

Applicants: Loi Nguyen
Ravishankar Sundaresan

Application No.:
Title: SRAM CELL FABRICATION WITH INTERLEVEL DIELECTRIC PLANARIZATION

Filing Date: January 20, 2000

Docket No.: 93-C-078C1-RE (1678-20)

REISSUE APPLICATION DECLARATION BY THE INVENTORS

As below-named inventors, we hereby declare that:

Our residence, post office address and citizenship are as stated below.

We believe that we are the original, first and joint inventors of the innovative subject matter described and claimed in the application for reissue of U.S. Patent No. 5,710,461 ('461 patent), which is entitled "SRAM CELL FABRICATION WITH INTERLEVEL DIELECTRIC PLANARIZATION," the specification of which is attached hereto.

We hereby state that we have reviewed and understand the contents of the above-identified U.S. reissue patent application, including both the original claims and the new claims presented in the enclosed First Preliminary Amendment.

We acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulation, § 1.56(a).

We believe the above-identified original '461 patent to be partly inoperative, by reason of the patentees claiming less than we had a right to claim. This error arose without any deceptive intention on our part.

Accordingly, the enclosed First Preliminary Amendment presents amended independent claims and additional dependent claims. These claims have been amended and drafted to more particularly point out and distinctly claim various aspects of our invention. We believe that our invention is at least as broad as these claims.

At least one error upon which reissue is based is described as follows. Issued claims 1 and 7 recite "a third patterned thin-film layer comprising substantially undoped polysilicon having a very high resistivity," and issued claim 12 recites "an additional patterned thin-film layer comprising substantially intrinsic polysilicon." Each of these thin film layers corresponds to layer in which resistors for a static random access memory (SRAM) cell are formed. Regarding these resistors, the specification expressly states in column 4, lines 46-51, that "[a]lthough the resistors are formed from intrinsic polysilicon in the presently preferred embodiment, it will be recognized that a slight amount of doping may be desirable to stabilize the characteristics of this material. For example, this material may be doped with chlorine, or may be SIPOS (containing a large fraction of oxygen)." Thus, the "substantially undoped" language unduly limits the scope of isued claims 1 and 7, and the same is true of the "substantially intrinsic" language in original claim 12.

As named inventors, we hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: LISA K. JORGENSON, Reg. No. 34,845; THEODORE E. GALANTHAY, Reg. No. 24,122; ROBERT D. MCCUTCHEON, Reg. No. 38,717; JEFF MOY, Reg. No. 39,307;and the attorneys associated with customer no. 000996 as follows: BRYAN A. SANTARELLI, Reg. No. 37,560; JEFFREY T. HALEY, Reg. No. 34,834; STEPHEN M. EVANS, Reg. No. 37,128; RICHARD O. GRAY, Reg. No. 26,550; PAUL F. RUSYN, Reg. No. 42,118; and, JOSHUA KING, Reg. No. 35,570.

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We do not know and do not believe that the claimed invention was ever known or used in the United States of America before our invention thereof.

We do not know and do not believe that the claimed invention was ever patented or described in any printed publication in any country before our invention thereof.

We do not know and do not believe that the claimed invention was ever patented or described in any printed publication in any country more than one year prior to the filing date of the original U.S. application.

We do not know and do not believe that the claimed invention was ever patented or made the subject of an inventor's certificate issued prior to the date of this application in any country foreign to the United States of America on an application filed by us or our legal representatives or assigns.

We do not know and do not believe that the claimed invention was ever in public use or on sale in the United States of America more than one year prior to the filing date of the original U.S. application.

We hereby declare that all statements made of our knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and may also jeopardize the validity of the application or any patent issued thereon.

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Date

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